Microelectronics Reliability 51 (2011) 207–211

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/microrel

AlGaN/GaN High Electron Mobility Transistor degradation under on- and off-state stress

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ARTICLE INFO

Article history:
Received 16 July 2010
Received in revised form 10 September 2010
Accepted 16 September 2010
Available online 8 October 2010

ABSTRACT

AlGaN/GaN High Electron Mobility Transistors (HEMTs) with various gate lengths have been step-stressed under both on- and off-state conditions. On-state, high power stress tests were performed on 0.17 μm gate length HEMTs and a single 5 μm spaced TLM pattern. Significant degradation of the submicron HEMTs as compared to the excellent stability of the TLM patterns under the same stress conditions reveal that the Schottky contact is the source of degradation. Off-state stress showed a linear relationship between the critical degradation voltage and gate length, though two dimensional ATLAS/Blaze simulations show that the maximum electric field is similar for all gate lengths. Additionally, as the drain bias was increased, the critical voltage decreased. However, the cumulative bias between the gate and drain remained constant, further indicating that the electric field is the main mechanism for degradation.

1. Introduction

GaN-based High Electron Mobility Transistors (HEMTs) have shown exceptional promise for use in both commercial and military systems for microwave and optoelectronic applications. Ultra-high power radar systems will require the use of GaN transistors to be operated at very high voltages, currents and temperatures. Though GaN HEMTs are emerging in the commercial market, there is still concern with respect to their electrical reliability and the driving mechanisms for degradation [1–8]. Numerous degradation mechanisms have been reported, ranging from hot-electron induced degradation to field-driven mechanisms [9–15]. High power operation of GaN HEMTs can also result in substantial self-heating, which will reduce the 2DEG mobility and saturation carrier velocity [16–19].

This paper reports on the degradation of AlGaN/GaN HEMTs under off-state (high reverse gate bias) and on-state (high power) conditions. The devices under test have a gate length ranging from submicron (0.1–0.17 μm) to 1 μm. To isolate the effect of the gate, a transmission line method structure was also stressed under the on-state condition. For the high power condition, both the source and gate were at ground while the drain was step-stressed. The effect of high reverse gate bias was investigated by step-stressing the gate from −10 V to −42 V with both source and drain at ground. Additional experiments were carried out to investigate the effect of applying drain bias while step-stressing the gate from −5 V to −42 V.

2. Experimental

The devices were fabricated on a semi-insulating 6H SiC substrate with an AlN nucleation layer, a 2.25 μm Fe-doped GaN buffer, and 15 nm $Al_{0.25}Ga_{0.75}N$ capped with 3 nm of unintentionally doped GaN. Hall measurements performed on-wafer displayed a sheet resistance of 310 Ohm/square, mobility of 1900 $cm^2/V\,s$, and sheet carrier concentration of $1.06 \times 10^{13}\ cm^{-2}$. Ohmic contacts of Ti/Al/Ni/Au were annealed for 30 s at 850 °C. The HEMTs employed a Ti/Au double gate design with a total gate width of 300 μm. All devices were passivated with SiN_X. The source-to-gate and gate-to-drain distances are 2 μm. Electrical data was measured by HP 4156C semiconductor parameter analyzer and an in-house designed stress system described elsewhere [20].

For the high power stress, both the source and gate were held at ground while the drain bias was stepped up in 1 V increments at 30 min intervals. HEMTs with a gate length of 0.17 μm (Fig. 1) were stressed with the base-plate temperature ranging from 60 °C to 100 °C. To examine the effect of the gate, a single TLM segment with a 5 μm ohmic to ohmic spacing and 90 μm width was stressed under the same conditions as the 0.17 μm gate length

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0026-2714/$ - see front matter © 2010 Elsevier Ltd. All rights reserved.
doi:10.1016/j.microrel.2010.09.024

Report Documentation Page

Form Approved
OMB No. 0704-0188

1. REPORT DATE	2. REPORT TYPE	3. DATES COVERED
2011		**00-00-2011 to 00-00-2011**

4. TITLE AND SUBTITLE	5a. CONTRACT NUMBER
AlGaN/GaN High Electron Mobility Transistor degradation under on- and off-state stress	5b. GRANT NUMBER
	5c. PROGRAM ELEMENT NUMBER
6. AUTHOR(S)	5d. PROJECT NUMBER
	5e. TASK NUMBER
	5f. WORK UNIT NUMBER
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) **University of Florida,Department of Materials Science and Engineering,Gainesville,FL,32611**	8. PERFORMING ORGANIZATION REPORT NUMBER
9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)	10. SPONSOR/MONITOR'S ACRONYM(S)
	11. SPONSOR/MONITOR'S REPORT NUMBER(S)

12. DISTRIBUTION/AVAILABILITY STATEMENT
Approved for public release; distribution unlimited

13. SUPPLEMENTARY NOTES

14. ABSTRACT

AlGaN/GaN High Electron Mobility Transistors (HEMTs) with various gate lengths have been stepstressed under both on- and off-state conditions. On-state, high power stress tests were performed on 0.17 lm gate length HEMTs and a single 5 lm spaced TLM pattern. Significant degradation of the submicron HEMTs as compared to the excellent stability of the TLM patterns under the same stress conditions reveal that the Schottky contact is the source of degradation. Off-state stress showed a linear relationship between the critical degradation voltage and gate length, though two dimensional ATLAS/Blaze simulations show that the maximum electric field is similar for all gate lengths. Additionally, as the drain bias was increased, the critical voltage decreased. However, the cumulative bias between the gate and drain remained constant, further indicating that the electric field is the main mechanism for degradation.

15. SUBJECT TERMS

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
a. REPORT	b. ABSTRACT	c. THIS PAGE			
unclassified	**unclassified**	**unclassified**	**Same as Report (SAR)**	**5**	

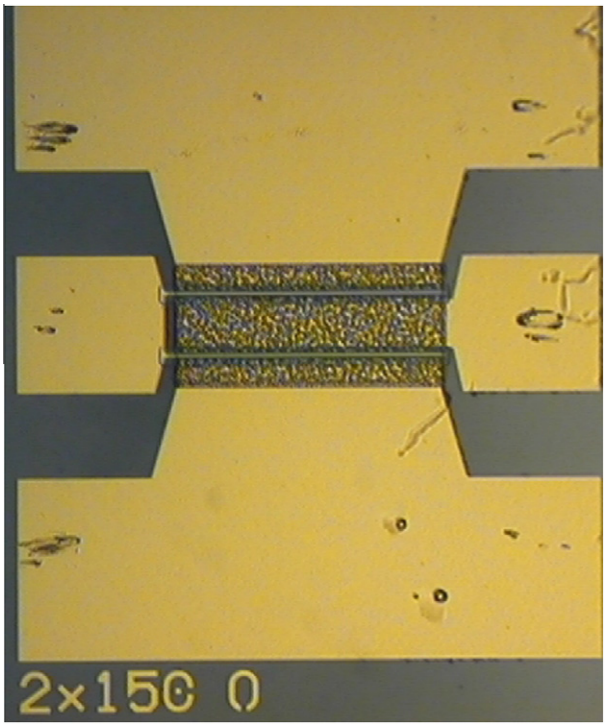

Fig. 1. Optical micrograph of AlGaN/GaN HEMT with double gate design.

HEMT. In order to investigate the effect of a high electric field on the gate while isolating any additional degradation due to self-heating, two additional sets of experiments were carried out on HEMTs with gate lengths of 0.1 μm, 0.125 μm, 0.14 μm, and 0.17 μm. The first test stepped V_{GS} from −10 V to −42 V in 1 V increments for 1 min intervals. Both the source and the drain were grounded, which allowed for symmetric stressing of the gate. The second test stepped a 0.1 μm gate from −5 V to −42 V in the same manner, with a drain bias of 0 V, 1 V, 5 V, 10 V and 15 V. In addition, finite element simulations were employed to estimate device channel temperature during operation. Automatically Tuned Linear Algebra Software (ATLAS/Blaze) simulations were also carried out in order to determine the electric field and theoretically confirm experimental results for the various gate lengths and bias conditions. Cross-sectional transmission electron microscopy (TEM) was performed on the devices pre- and post-stress.

3. Results and discussion

3.1. On-state stress

HEMTs with a gate length of 0.17 μm were step-stressed with a drain bias of 1 V to 25 V. A positive shift in V_T of ~0.5 V was observed at 60 °C and an increase in V_T of ~0.7 V at 100 °C. As evident in the top of Fig. 2, an increase in base-plate temperature of 40 °C results in ~15% decrease in I_{DSS} during the stress test. Upon closer inspection of the drain current (bottom of Fig. 2), the output current is constant for the duration of each step until a critical voltage is applied, at which point the degradation becomes permanent in nature and the output current decays under constant drain bias. This permanent degradation occurs when 10 V and 13 V is applied on the drain for a base-plate temperature of 100 °C and 60 °C, respectively. The channel temperature at the onset of degradation for both base-plate temperatures is 195 °C, as determined by three dimensional finite element thermal simulations. The maximum temperature in the channel during the stress test was 240 °C for

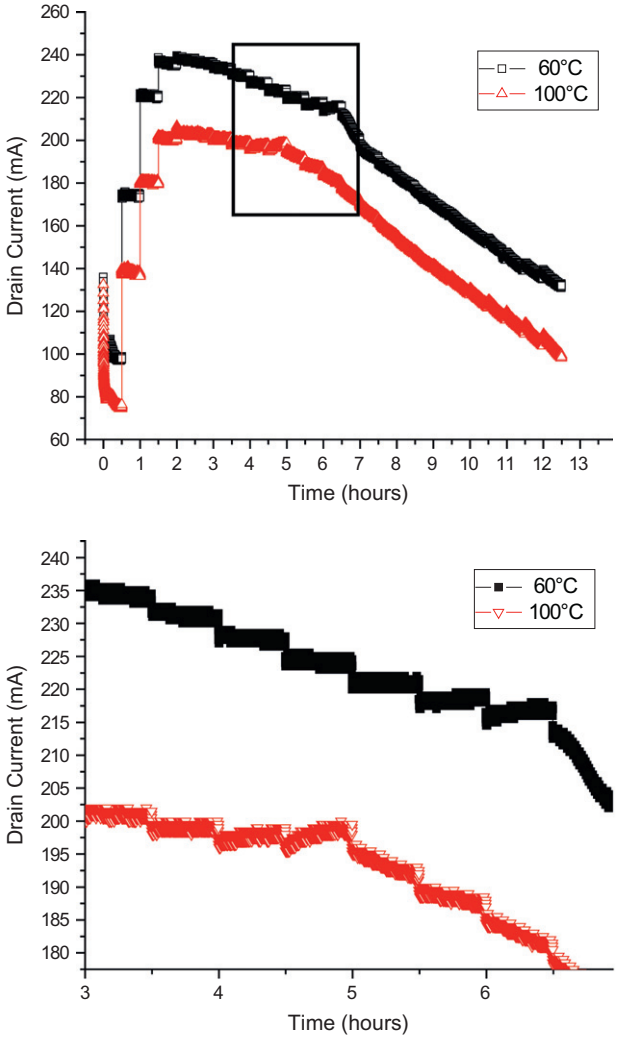

Fig. 2. (Top) Drain current of 0.17 μm gate length HEMT during step stress with base-plate temperatures of 60 °C and 100 °C. (Bottom) Enlarged section of drain current shown in top figure.

both base-plate temperatures. These results show that degradation is due to a temperature activated mechanism. Both base-plate temperatures resulted in ~90% decrease in drain current. Additionally, gate current characteristics after stress show about a two orders of magnitude increase in leakage current for a base-plate temperature of 60 °C, and about three orders of magnitude increase at 100 °C (Fig. 3). In order to eliminate the effect of the gate on the device, transmission line method (TLM) patterns with a 5 μm spacing were also stressed under the same conditions. Though the drain current for the HEMT devices exhibited substantial degradation at a lower current density, the TLM patterns exhibited excellent stability regardless of the base-plate temperature, with negligible increase in total resistance (Fig. 4 top). In addition, the sheet resistance was found to be independent of temperature (Fig. 4 bottom), further establishing that the ohmic contacts and underlying epitaxial layers are not the source of degradation in the HEMTs.

3.2. Off-state stress with V_{DS} = 0V

AlGaN/GaN HEMTs with submicron gate lengths were step-stressed with a gate bias of −10 V to −42 V in 1 V increments for 1 min at each voltage step with both source and drain at ground. The current during stress ($I_{Gstress}$) steadily increases with time,

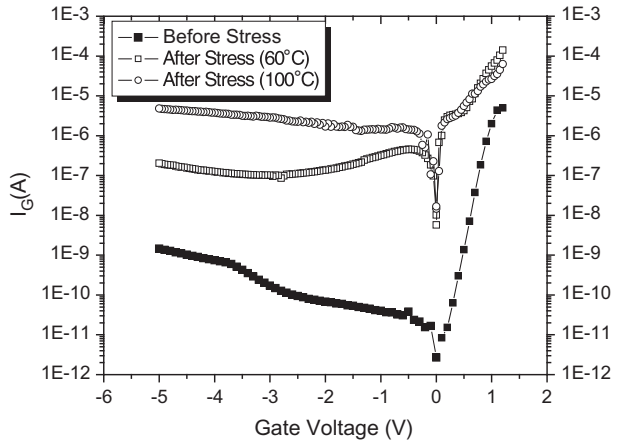

Fig. 3. Gate current of 0.17 μm gate length HEMT before and after on-state step stress with a base-plate temperature of 60 °C and 100 °C.

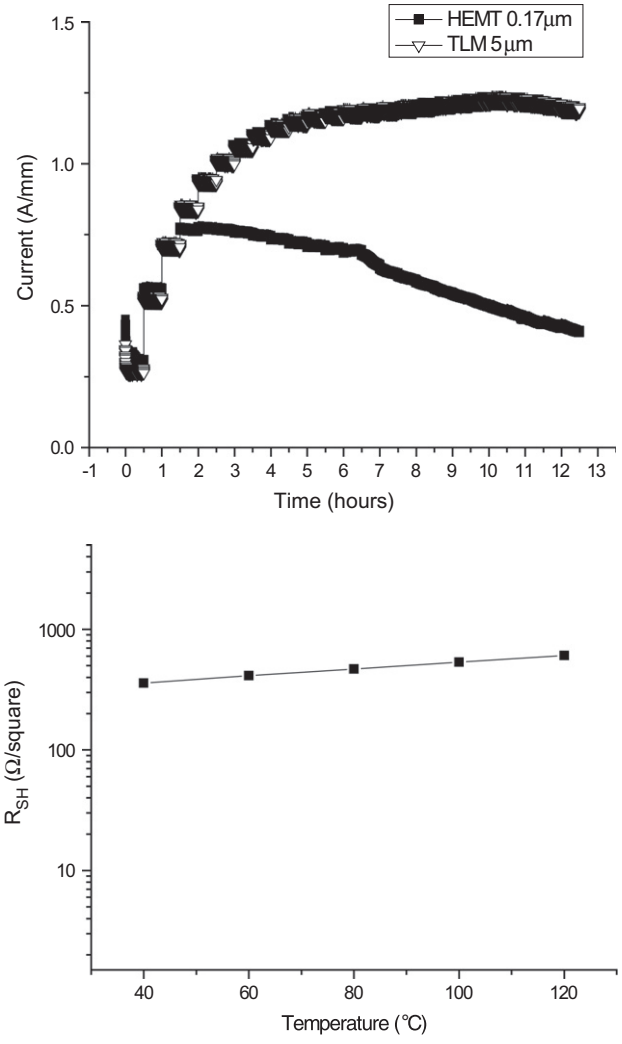

Fig. 4. (Top) Comparison of current (A/mm) of 0.17 μm gate length HEMT and TLM with 5 μm spacing. (Bottom) Temperature dependence of sheet resistance.

until at a certain applied voltage, $I_{Gstress}$ abruptly rises up about one order of magnitude. This has been deemed the critical voltage (V_{crit}). The V_{crit} for 100 nm, 125 nm, 140 nm and 170 nm gate lengths was determined to be −17 V, −22 V, −27 V and −32 V, respectively (Fig. 5). Two dimensional ATLAS/Blaze simulations were carried out in order to determine the electric field strength at the critical voltage for each of the gate lengths (top of Fig. 6). As seen in the bottom of Fig. 6, the critical voltage is linearly dependent on gate length. However, the electric field is fairly similar at all gate lengths when the critical voltage is reached, ~1.9 MV/cm to ~2.7 MV/cm.

The gate current before and after stress for the 140 nm gate length device is shown in Fig. 7 (top). Prior to stress, there is an

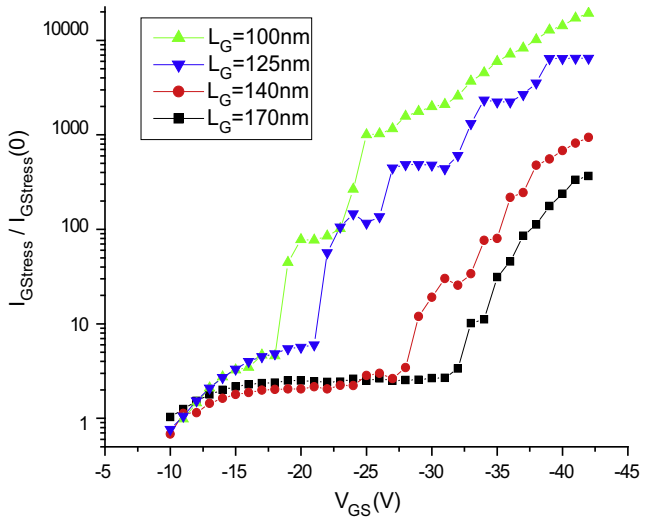

Fig. 5. Stress gate current ($I_{Gstress}$) and stress voltage with V_{DS} = 0 for reverse gate bias step-stress experiment for different gate length devices.

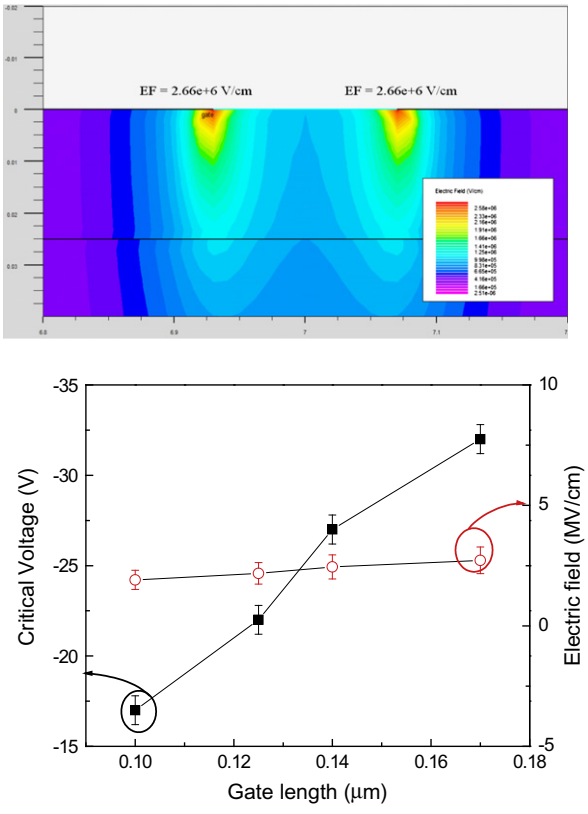

Fig. 6. (Top) ATLAS/BLAZE simulation of electric field at the critical voltage for the 0.14 μm gate length HEMT at 300 K. (Bottom) Simulated maximum electric field as a function of gate length.

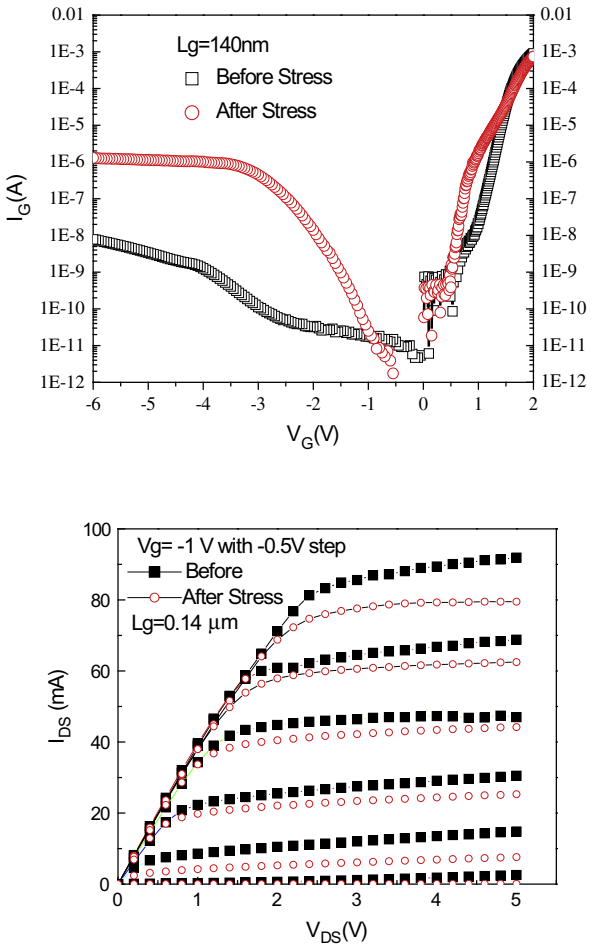

Fig. 7. (Top) Gate current of 0.14 μm gate length device before and after gate step stress from −10 V to −42 V. (Bottom) Drain current as a function of drain voltage for 0.14 μm gate length HEMT before and after DC stress.

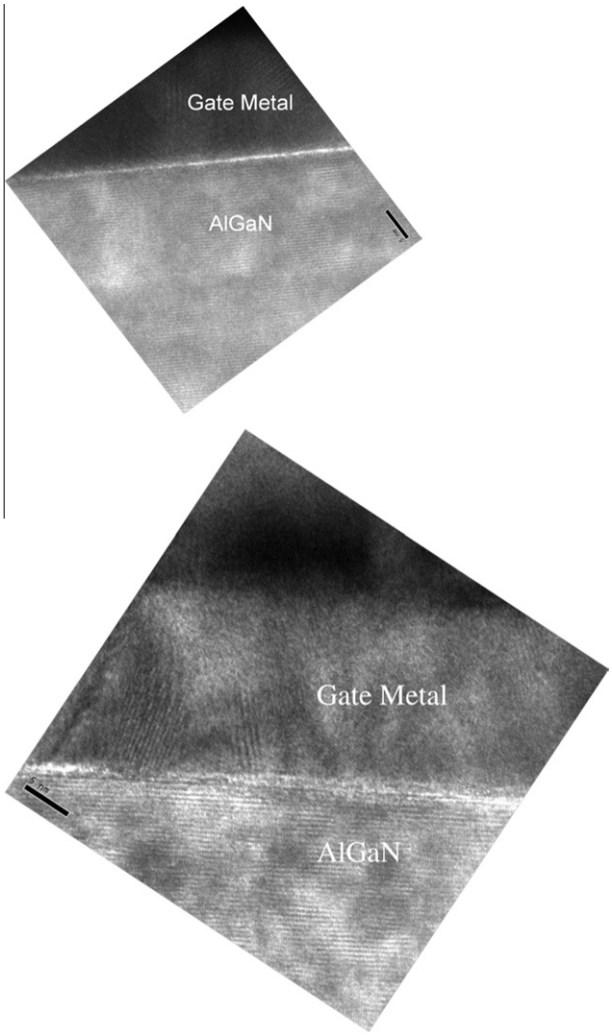

Fig. 8. Cross-sectional TEM image of gate finger (top) before and (bottom) after off-state stress.

anomalous current plateau present in the forward *I–V* curve. A high density of spatially non-uniform surface donors with both thermionic field emission and field emission current transport has been reported by Hasegawa and Oyama as the thin surface barrier model [21]. Though unintentional, the thin surface barrier results in a current plateau and may be present in our devices due to a defective nitride with a high dislocation density. After stress, the reverse gate current increases an order of magnitude and the forward current begins to show normal Schottky transport. As seen in the bottom of Fig. 7, the drain current decreases ~10% after stress. The Schottky barrier height also reduces from ~800 mV to ~770 mV, indicating that the interface between the semiconductor and the gate metal is changing. Cross-sectional TEM before stress shows a thin oxide layer present at the interface, which is reduced after stress (Fig. 8). As the devices are stressed beyond the critical voltage, plateaus in $I_{Gstress}$ form and can be seen in Fig. 5, particularly in the smaller gate length HEMTs. These plateaus are followed by less significant increases in stress current.

3.3. Off-state stress with drain–source bias

V_{GS} for HEMTs with a 0.1 μm gate length was stepped from −5 to −42 V in 1 V increments for 1 min at each interval with drain voltages ranging from 0 V to 15 V. The changes in $I_{Gstress}$ for the various values of V_{DS} are shown in Fig. 9. As shown in Fig. 10, as drain bias is increased, the critical voltage significantly decreases.

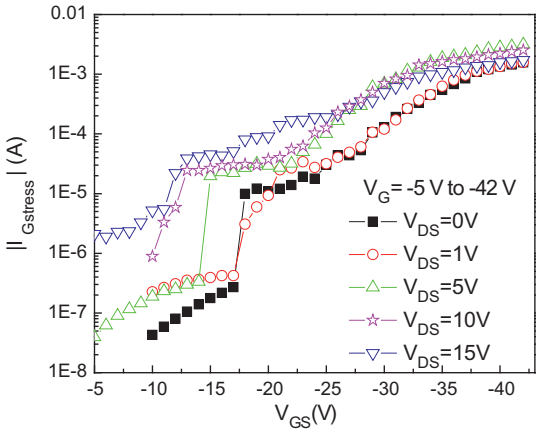

Fig. 9. $I_{Gstress}$ for reverse gate bias step-stress experiments at various drain bias.

The voltage applied between the drain and gate ($|V_{GS}| + V_{DS}$) when gate current degradation occurs, however, is almost constant (Fig. 10). This result further shows that the electric field between the drain and gate is the primary cause of degradation.

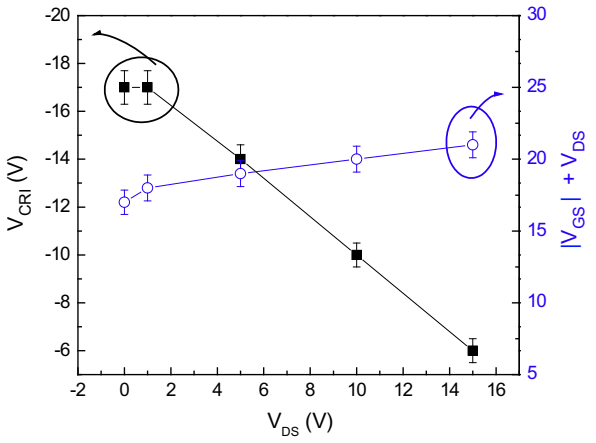

Fig. 10. Critical voltage and total voltage between gate and drain (V_{DG}) as function of applied drain voltage for reverse gate bias stress test.

4. Summary and conclusions

AlGaN/GaN HEMTs with a gate length of 0.17 μm and TLM patterns with a 5 μm spacing were step-stressed under on-state, high power conditions. Devices with 0.17 μm gate length exhibited the onset of degradation at lower voltages with an increase in baseplate temperature. Thermal simulations, however, showed that permanent degradation occurred at the same channel temperature. Both gate and drain current–voltage characteristics reveal significant degradation, while the TLM structure displays remarkable stability under the same stress conditions and higher current density. These results confirm that the Schottky contact is the source of degradation for the HEMT. Reaction of the gate with the underlying epitaxial layers and subsequent gate metal sinking would result in a decrease in distance between the metal–semiconductor interface and the channel. This sinking would in turn increase the depletion region and account for the decrease in drain current, increase in V_T, and an increase in gate leakage current seen in the HEMTs.

The effect of off-state conditions was investigated for submicron gate length HEMTs. Due to the low currents under these conditions, self-heating did not occur. For $V_{DS} = 0$, a linear relationship between gate length and critical voltage was observed. Step-like increases in current reveal that the reaction occurring between the gate and underlying semiconductor layers is not a single, instantaneous event, but rather an incremental process. Chowdhury et al. performed an extensive TEM investigation of electrically stressed GaN HEMTs to study the inverse piezoelectric effect [15]. Analysis showed a correlation between electrical degradation and physical degradation, with small pits forming on the drain side of the gate after modest electrical degradation and large cracks with gate metal diffusion after significant electrical degradation [15]. While our samples did not reveal pit or crack formation after stressing, physical degradation of the Schottky contact is apparent and future studies will further investigate the evolution of gate degradation. Additional experiments investigated the effect of increasing drain bias from 0 V to 15 V while step-stressing the gate from −5 V to −42 V resulted in a decrease in V_{crit}. However, the total applied voltage between the gate and the drain, $|V_{GS}| + V_{DS}$, remained almost constant. Simulations showed the electric field strength for all gate lengths at the critical voltage was similar, demonstrating that the field is the dominant degradation mechanism under off-state stress.

Acknowledgments

This work is supported by an AFOSR MURI monitored by Gregg Jessen.

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